CLAIMS

What is claimed is:

1. A semiconductor package comprising:

a semiconductor die comprising an active surface with bond pads thereon, an opposite inactive surface, and four peripheral side surfaces extending between the active and inactive surfaces;

a substrate comprising a first surface, a second surface opposite and parallel to the first surface, a third surface extending between the first and second surfaces, and conductive circuit patterns at the second and third surfaces,

wherein the first surface of the substrate is coupled to only a first one of the four peripheral side surfaces of the semiconductor die, the third surface of the semiconductor die is coplanar with the active surface of the semiconductor die, and the bond pads of the semiconductor die are electrically coupled to the conductive circuit patterns of the third surface of the substrate; and

external interconnects electrically coupled to the circuit patterns of the second surface of the substrate, whereby at least some of the external interconnects are electrically coupled to the semiconductor die.

2. The semiconductor package of claim 1, wherein the circuit patterns of the second surface of the substrate include ball lands, and the external interconnects are solder balls.

3. The semiconductor package of claim 1, wherein the circuit patterns of the third surface of the substrate include bond fingers, and the bond pads of the semiconductor die are electrically coupled to the bond fingers by conductive wires.

4. The semiconductor package of claim 3, further comprising an insulative encapsulant covering the active surface of the semiconductor die, the conductive wires, and the third surface of the substrate.

5. The semiconductor package of claim 4, wherein the encapsulant includes opposed parallel first and second surfaces, with the first surface being coplanar with a second of the side surfaces of the semiconductor die that is opposite to the first side surface of the semiconductor die, and with the second surface of the encapsulant being coplanar with the second surface of the substrate.

6. The semiconductor package of claim 1, wherein the circuit patterns of the second surface of the substrate are electrically coupled to the circuit patterns of the third surface of the substrate by vias extending through an insulative core of the substrate between the second and third surfaces.

7. The semiconductor package of claim 1, wherein the circuit patterns of the second surface of the substrate are electrically coupled to the circuit patterns of the third surface of the substrate by circuit patterns extending over the second and third surfaces of the substrate.

8. The semiconductor package of claim 1, further comprising a first insulating layer covering the active surface of the semiconductor die and the third surface of the substrate, a second insulating layer covering the first insulating layer, and conductive first circuit patterns extending through the first and second insulating layers,

wherein the bond pads of the semiconductor die are electrically coupled to the circuit patterns of the third surface of the substrate through the first circuit patterns.

9. The semiconductor package of claim 8, wherein a surface of the first circuit patterns is exposed through an outer surface of the second insulating layer.

10. The semiconductor package of claim 1, wherein the active surface of the semiconductor die and the third surface of the substrate are together covered by a layer of an insulating material, and the inactive surface and the remaining three of the four side surfaces of the semiconductor die are exposed.

11. A semiconductor package comprising:

a semiconductor die comprising an active surface with bond pads thereon, an opposite inactive surface, and four peripheral side surfaces extending between the active and inactive surfaces;

first and second substrates each comprising a first surface, a second surface opposite and parallel to the first surface, a third surface extending between the first and second surfaces, and conductive circuit patterns at the first and second surfaces,

wherein the third surface of the first substrate is coupled only to a first of the four side surfaces of the semiconductor die, the third surface of the second substrate is coupled only to a second of the four side surfaces of the semiconductor die, the second side surface being opposite to the first side surface, and the first surface of each of the two substrates is coplanar with the active surface of the semiconductor die,

wherein the circuit patterns of the first surface of the first and second substrates are electrically coupled to the circuit patterns of the second surface of the respective substrate, and

wherein some of the bond pads of the semiconductor die are electrically coupled to the circuit patterns of the first surface of the first substrate, and some of the bond pads of the semiconductor die are electrically coupled to the circuit patterns of the first surface of the second substrate; and

external interconnects electrically coupled to the circuit patterns of the second surface of the first and substrates, whereby the external interconnects of the first and second substrates are electrically coupled to the semiconductor die.

12. The semiconductor package of claim 11, wherein the circuit patterns of the second surface of the first and second substrates include ball lands, and the external interconnects are solder balls.

13. The semiconductor package of claim 11, wherein the circuit patterns of the first surface of the first and second substrates include bond fingers, and the bond pads of

the semiconductor die are electrically coupled to the bond fingers of the first and second substrates by conductive wires.

14. The semiconductor package of claim 13, further comprising an insulative encapsulant covering the active surface of the semiconductor die, the conductive wires, and the first surface of the first and second substrates.

15. The semiconductor package of claim 11, wherein the circuit patterns of the first surface of the first and second substrates are electrically coupled to the circuit patterns of the second surface of the respective substrate by vias extending through an insulative core of the substrate between the first and second surfaces.

16. The semiconductor package of claim 1, wherein the circuit patterns of the first surface of the first and second substrates are electrically coupled to the circuit patterns of the second surface of the substrate by circuit patterns extending over a fourth surface of the substrate that is parallel to and opposite the third surface of the substrate.

17. The semiconductor package of claim 1, further comprising a first insulating layer covering the active surface of the semiconductor die and the third surface of the first and second substrates, a second insulating layer covering the first insulating layer, and conductive first circuit patterns extending through the first and second insulating layers,

wherein the bond pads of the semiconductor die are electrically coupled to the circuit patterns of the third surface of the first and second substrates through the first circuit patterns.

18. The semiconductor package of claim 17, wherein a surface of the first circuit patterns is exposed through an outer surface of the second insulating layer.

19. The semiconductor package of claim 11, wherein the active surface of the semiconductor die and the third surface of the substrate are together covered by a layer of

an insulating material, and the inactive surface and the remaining two of the four side surfaces of the semiconductor die are exposed.

20. A semiconductor package comprising:

a semiconductor die comprising an active surface with bond pads thereon, an opposite inactive surface, and four peripheral side surfaces extending between the active and inactive surfaces;

first and second substrates each comprising a first surface, a second surface opposite and parallel to the first surface, a third surface extending between the first and second surfaces, and conductive circuit patterns at the first and second surfaces,

wherein the third surface of the first substrate is coupled only to a first of the four side surfaces of the semiconductor die, the third surface of the second substrate is coupled only to a second of the four side surfaces of the semiconductor die, with the second side surface being opposite and parallel to the first side surface of the semiconductor die, and the first surface of the first and second substrates is coplanar with the active surface of the semiconductor die,

wherein at least some of the circuit patterns of the first surface of the first and second substrates are electrically coupled through the respective substrate to at least some of the circuit patterns of the second surface of the substrate, and

wherein some of the bond pads of the semiconductor die are electrically coupled by bond wires to the circuit patterns of the first surface of the first substrate, and some of the bond pads of the semiconductor die are electrically coupled by bond wires to the circuit patterns of the first surface of the second substrate;

solder balls electrically coupled to the circuit patterns of the second surface of the first and substrates, whereby the solder balls of the first and second substrates are electrically coupled to the semiconductor die; and

a layer of an encapsulant overlying the active surface of the semiconductor die, the bond wires, and the first surface of the first and second substrates,

wherein the inactive surface of the semiconductor die and the remaining two of the four side surfaces of the semiconductor die are exposed.